NASA CR-143825

SCHEMATICS

for

MAN-COMPUTER INTERACTIVE DATA
ACCESS SYSTEM (McIDAS)

Final Report on Contract NAS5-23296

BOOK 1

(NASA-CR-143825) SCHEMATICS FOR MAN-COMPUTER INTERACTIVE DATA ACCESS SYSTEM (MCIDAS), BOOK 1 Final Report (Wisconsin Univ.) 198 p HC $7.00 CSCI 09B G3/60

N75-28734

Unclas 31273

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

THE UNIVERSITY OF WISCONSIN

SPACE SCIENCE & ENGINEERING CENTER

MADISON, WISCONSIN

TITLE

McIDAS VIDEO CHAIN
DRAWING LIST

SCALE	DRAFTSMAN	DATE	CHECKER
None	WBL	March 75	
NEXT HIGHER ASSEMBLY		PRODUCT ASSURANCE	
PROJECT NO. 7001	SIZE A	SHEET 1 OF 2	DRAWING

McIDAS Video Chain
Drawing List

7001-2001

DRAWING NO.	SIZE	TITLE	DATE
7001-2001	A	McIDAS Video Chain Drawing List	March 75
7001-2002	D	McIDAS Video Chain Detailed Functional Block Diagram	March 75
7001-2003	E	McIDAS Unit Interface	March 75
7001-2004	E	Digital Interface Control	March 75
7001-2005	E	Digital Interface Latch Detail	March 75
7001-2006	E	Fast Storage	March 75
7001-2007	D	DR-10A Interface	March 75
7001-2008	D	DR-10A Disc Monitor	March 75
7001-2009	E	Enhancement Table (2 Drawing Set)	March 75
7001-2010	D	Analog Distributor	March 75
7001-2011	D	Address Multiplexer	March 75
7001-2012	D	Digital Multiplexer	March 75
7001-2013	D	Video Sequencer	March 75
7001-2014	D	Timing Generator	March 75
7001-2015	E	Digital Cursor	March 75
7001-2016	E	Level Discriminator	March 75
7001-2017	D	Subsystem Interconnection Diagram Cabinet #1	March 75
7001-2018	D	Subsystem Interconnection Diagram Cabinet #2	March 75
7001-2019	D	Data Injestion System	March 75
7001-2020	D	Data Injestion System Data Package Module	March 75

REVISION

DRAWING NO. 7001-2001

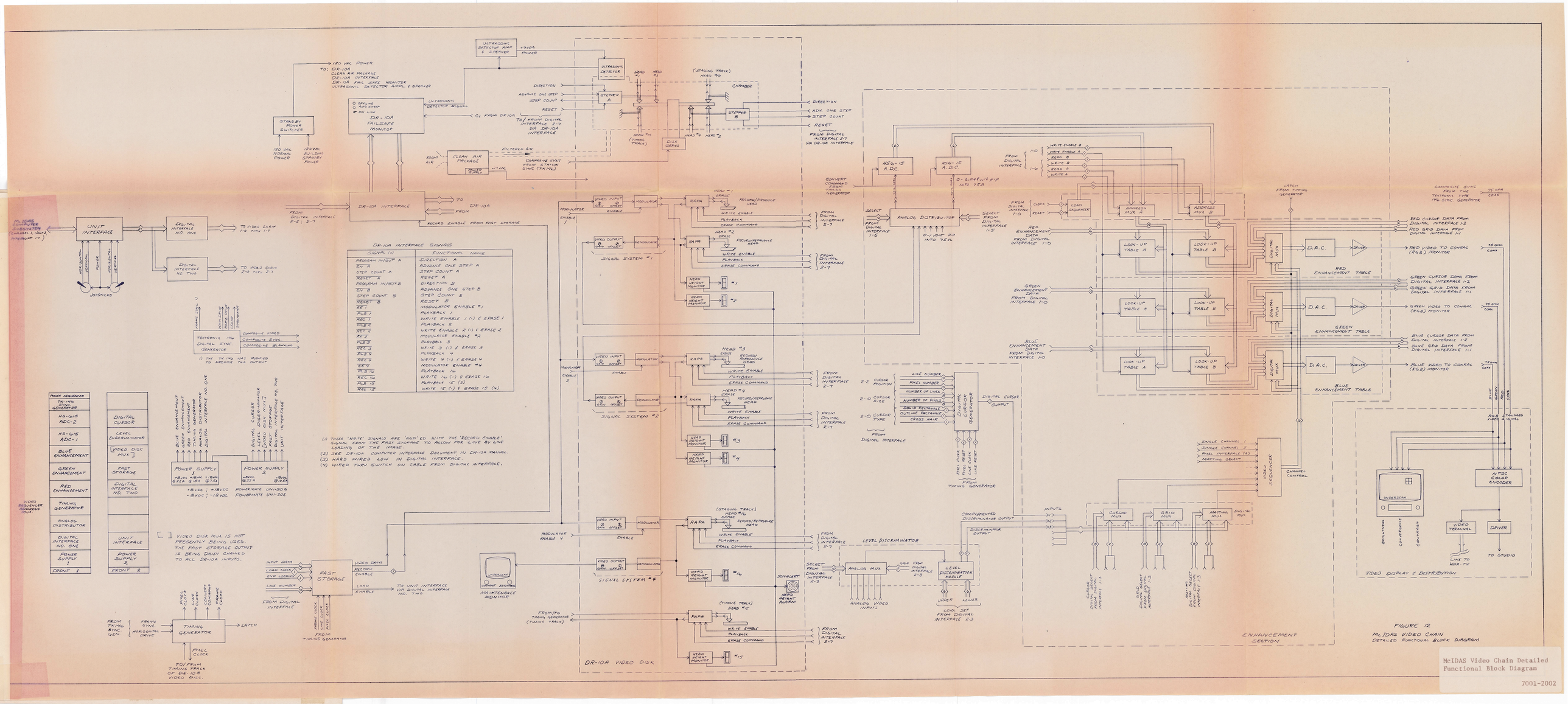

FIGURE 12
McIDAS VIDEO CHAIN
DETAILED FUNCTIONAL BLOCK DIAGRAM

McIDAS Video Chain Detailed Functional Block Diagram

7001-2002

SUBSYSTEM CONTROL BITS
(TO ALL DIGITAL INTERFACES VIA DAISY CHAIN)

COMPUTER LOAD CLOCK (TO ALL DIGITAL INTERFACES VIA DAISY CHAIN)

IMPORTANT
SEE NOTE #3

+5V

(15A-9) DFC 00+
(15A-13) DFC 01+
(16A-7) DFC 02+
(16A-9) DFC 03+
(16A-13) DFC 04+
(17A-7) DFC 05+
(17A-9) DFC 06+
(17A-13) DFC 07+
(1A-7) DFC 08+
(1A-9) DFC 09+
(1A-13) DFC 10+
(2A-7) DFC 11+
(2A-9) DFC 12+
(2A-13) DFC 13+

(3A-7) DFC 14+
(3A-9) DFC 15+
(3A-13) DFC 16+
(4A-7) DFC 17+
(4A-9) DFC 18+
(4A-13) DFC 19+
(5A-7) DFC 20+
(5A-9) DFC 21+
(5A-13) DFC 22+
(12A-7) DFC 23+

36C1024 17C

WORD ADDRESS WEIGHT 1
WORD ADDRESS WEIGHT 2
WORD ADDRESS WEIGHT 4
DIGITAL INTERFACE NO. FOUR SELECT
DIGITAL INTERFACE NO. THREE SELECT
DIGITAL INTERFACE NO. TWO SELECT
DIGITAL INTERFACE NO. ONE SELECT

(TO ALL DIGITAL INTERFACES VIA DAISY CHAIN)

8202 — 1G
8202 — 2G

A0 DIGITAL MUX ADDRESS
A1
A2
(TO DATA INJESTION SYSTEM)

COMMAND LATCH
300 pf

CONVERT COMMAND
ANALOG MUX ADDRESS

(11A-5) DATC +
OUTPUT DATA ACCEPTED (TO COMPUTER)

(15A-7) O-DDHG +
OUTPUT DATA HERE (FROM COMPUTER)

(14A-13) O-CDHG +
COMMAND DATA HERE (FROM COMPUTER)

3C (P.N. 16 +5)
SEE NOTE #1

τ = 200 nsec
30pf 10K
(SEE 3C(B))
5D
8T22

τ = 5 μ sec
1500pf 10K
(SEE 3C(A))
6D
8T22
ENABLE

(18-5) EII +
INPUT INTERRUPT (TO COMPUTER)

(12B-5) IDAV +
INPUT DATA AVAILABLE (TO COMPUTER)

(14A-9) DATC +
INPUT DATA ACCEPTED (FROM COMPUTER)

MC3000

2D
3060

τ = 1 μsec
240pf 10K
(SEE 3C(C))
10D
8T22

INTERRUPT

N7374

NO LONGER USED 3-17-75

THIS CONFIGURATION IS TO ALLOW THE 'OR'ING OF MULTIPLE SIGNALS AS INTERRUPTS

P19-C19
FRAME SYNC
(FROM TIMING UNIT (TIMING GENERATOR))

DIGITIZED DATA (TO COMPUTER)

DIGITAL OUTPUT

DATEL DAS-16M DATA ACQUISITION SYSTEM

SHORT CYCLE
BUSY
RANDOM/SEQUENTIAL
DEVICE SELECT
CONVERT COMMAND
RESET
STROBE ANALOG MUX ADDRESS

ANALOG INPUTS (CHANNEL NO.)

ANALOG INPUTS (FROM REAR PANEL BNC CONNECTOR)

NOTE: NEGATIVE LOGIC

MASTER CLEAR
(TO DIGITAL INTERFACE VIA DAISY CHAIN)

+18V (FROM POWER SUPPLY)
MC1468
+15V REG.
COAX P2
COAX P3
JOYSTICK TWO
JOYSTICK ONE
VERTICAL
HORIZONTAL

DAS-16M
CHANNEL 3
CHANNEL 1
CHANNEL 2
CHANNEL 4

CAPACITOR IS NEEDED TO REDUCE NOISE. ZENERS ARE SELECTED TO CLAMP INPUT AT 10.0 VOLTS TO KEEP EXCESS VOLTAGES FROM "BLEEDING" OVER INTO OTHER CHANNELS.

2C
2N4401

(01M-6) ICB+
MASTER CLEAR (FROM COMPUTER)

ANALOG CHANNEL

CHANNEL NUMBER	INPUT
1	JOYSTICK Y P19-2
2	SPARE
3	JOYSTICK X P19-1
4	SPARE
5	DATA INJESTION #2
6	DATA INJESTION #1
7	——
8	——
9	——
10	——
11	——
12	——
13	——
14	——
15	——
16	——

NOTES:
1. PIN 8 OF CARRIER 3C MUST BE PHYSICALLY CUT OFF TO PREVENT SHORTING OF THE SIGNAL TO GROUND.
2. COMPUTER MUST WAIT UNTIL IT RECEIVES AN IDAV+ SIGNAL AFTER IT SENDS A CONVERT COMMAND BEFORE IT SENDS A SECOND CONVERT COMMAND.
3. PULL-UP RESISTORS ARE 16 PIN DIP PACKAGES LOCATED AT 6C, 7C, 8C & 9C. PACKAGE IS THE 36C1024 WHICH CONTAIN 1K OHM RESISTORS AND NOT THE 820 OHM SHOWN. THE CORRECT VALUE WILL BE SUBSTITUTED WHEN THEY BECOME AVAILABLE.

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MADISON, WISCONSIN

TITLE: McIDAS UNIT INTERFACE

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
NONE	JRD	1/8/74				
NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE	DATE	PROJECT APPROVAL	DATE		
PROJECT NO. 5010	SIZE E	SHEET 1 OF 1	DRAWING NO.			

McIDAS Unit Interface
7001-2003

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

MODE SELECT (FROM MODE SWITCH) S_1 S_0

S_0	S_1	
1	1	COMPUTER
0	1	MANUAL
1	0	EXTERNAL
0	0	ALL OUTPUTS '0'

N8250

D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

IF D IS '1' CHIP IS DE-SELECTED

LOAD CLOCK (FROM MODE SWITCH)

MASTER CLEAR (FROM COMPUTER OR RESET BUTTON VIA MODE SWITCH) [LOW TO RESET]

WORD ADDRESS (FROM UNIT INTERFACE) (FROM EXTERNAL) (FROM MANUAL CONTROL)

WEIGHT 4 2 1

BLU/BLK GRN/BLK YEL/BLK

[TO BE ADDED LATER IF DESIRED]

B263 G

B250 A

WORD 0 [NEGATIVE LOGIC]

1K +5

PACKAGE SELECT (FROM UNIT INTERFACE) (FROM EXTERNAL) (FROM MANUAL CONTROL)

B263 H

DIGITAL INTERFACE

NEGATIVE LOGIC

WIRE THIS TO SPECIFY EACH BOARD

PACKAGE DESIGNATION WIRING

N8885 N8885

270pf 270pf 270pf 270pf 207pf 207pf 207pf

COMPUTER WORD LATCHES

WORD CLOCK

WORD NUMBER 0 — 24 BITS
WORD NUMBER 1 — 24 BITS
WORD NUMBER 2 — 24 BITS
WORD NUMBER 3 — 24 BITS
WORD NUMBER 4 — 24 BITS
WORD NUMBER 5 — 24 BITS
WORD NUMBER 6 — 24 BITS
WORD NUMBER 7 — 24 BITS

CONTROL BITS (TO HARDWARE SUBSYSTEMS)

τ = 100 n SEC 62 pf 10K +5

BT22 A

BLU/BLK

BRN/BLK COMPUTER LOAD CLOCK (TO MODE SWITCH)

MANUAL LOAD CLOCK (TO MODE SWITCH)

VIO/BLK

MC3060 [NON BOUNCE FLIP FLOP]

SET RESET (FROM MANUAL LOAD SWITCH)

OUTPUT DATA AVAILABLE (ODH+) (FROM UNIT INTERFACE)

24 POLE, 3 POSITION DIGITAL MULTIPLEXER

MODE SELECT (FROM MODE SELECT)

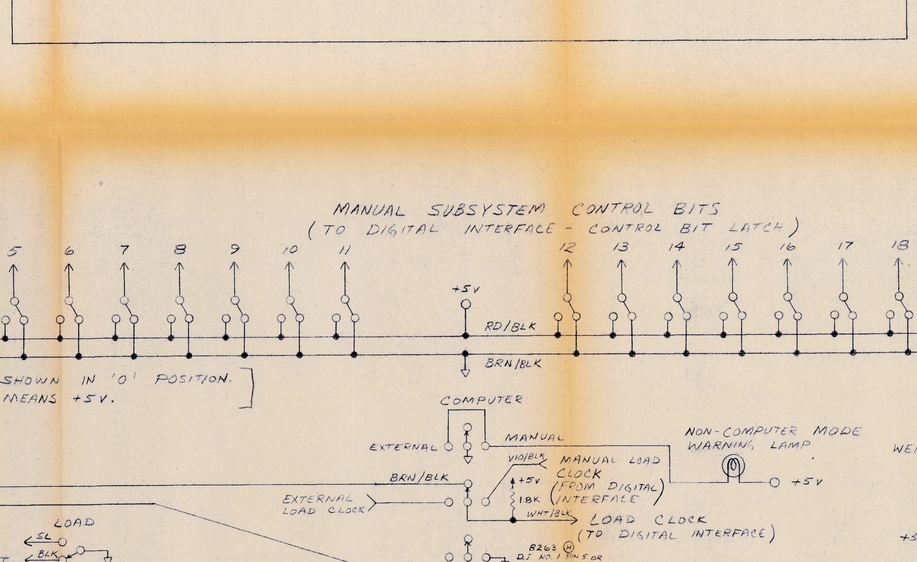
(FROM UNIT INTERFACE) 24 BITS

(FROM MANUAL CONTROL SWITCHES) 24 BITS

(FROM EXTERNAL TO BE ADDED LATER IF DESIRED) 24 BITS

(FROM UNIT INTERFACE) GRN/BLK → COMPUTER MASTER CLEAR (TO MODE SWITCH)
[DIRECT WIRED]

DIGITAL INTERFACE FRONT PANEL



MANUAL SUBSYSTEM CONTROL BITS
(TO DIGITAL INTERFACE - CONTROL BIT LATCH)

BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23

+5V RD/BLK BRN/BLK

[ALL BIT SWITCHES SHOWN IN '0' POSITION. '0' MEANS GND. '1' MEANS +5V.]

COMPUTER LOAD CLOCK FROM UNIT INTERFACE

RESET

LOAD SET RESET SL BLK (TO DIGITAL INTERFACE (NON-BOUNCE FLIP FLOP))

[MOMENTARY SWITCH SHOWN IN NON-ACTIVATED POSITION]

[MOMENTARY SWITCH SHOWN IN NON-ACTIVATED POSITION]

COMPUTER MASTER CLEAR (FROM UNIT INTERFACE)

COMPUTER EXTERNAL MANUAL

BRN/BLK EXTERNAL LOAD CLOCK

VIO/BLK MANUAL LOAD CLOCK (FROM DIGITAL INTERFACE)

+5V 1.8K WHT/BLK LOAD CLOCK (TO DIGITAL INTERFACE)

NON-COMPUTER MODE WARNING LAMP +5V

B263 (H) DI NO. 1 PIN 5 OR DI NO. 2 PIN 2 RD/BLK PACKAGE SELECT (TO DIGITAL INTERFACE)

+5V 1K ORG/BLK MASTER CLEAR (TO DIGITAL INTERFACE)

+5V

+5V BLK S_1 VEL S_0 MODE SELECT (TO DIGITAL INTERFACE)

MODE SWITCH (6 POLE, 3 POSITION)

MANUAL WORD ADDRESS (TO DIGITAL INTERFACE)

WEIGHT 4 2 1

+5V YEL/BLK GRN/BLK BLU/BLK

[SWITCHES SHOWN IN '0' POSITION '0' MEANS GND. '1' MEANS +5V.]

THE UNIVERSITY OF WISCONSIN SPACE SCIENCE & ENGINEERING CENTER MADISON, WISCONSIN							
TITLE: McIDAS DIGITAL INTERFACE CONTROL							
SCALE NONE	DRAFTSMAN DW	DATE 11/3/74	CHECKER	DATE	ENGINEER	DATE	
NEXT HIGHER ASSEMBLY		PRODUCT ASSURANCE	DAT				
PROJECT NO. 5010	SIZE E	SHEET 1 OF 2	DRAWING NO.				

Digital Interface Control
7001-2004

5010-0008 S 9 5

DIGILAB INTERFACE

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

SUBSYSTEM CONTROL WORDS (FROM UNIT INTERFACE) (FROM MANUAL CONTROL SWITCHES)

MODE SELECT (FROM MODE SWITCH) S_1 S_0

S_0 PIN 17	S_1 PIN 6	
1	1	COMPUTER
0	1	MANUAL
1	0	EXTERNAL
0	0	ALL OUTPUTS '0'

WORD CLOCK

MASTER CLEAR (SETS ALL OUTPUTS TO '0')

SEE NOTE ONE

8263 MULTIPLEXER — BIT 0 — (FROM EXTERNAL) TO BE ADDED LATER IF DESIRED

8263 MULTIPLEXER — BIT 4 — (FROM EXTERNAL) TO BE ADDED LATER IF DESIRED

8263 MULTIPLEXER — BIT 8 — (FROM EXTERNAL) TO BE ADDED LATER IF DESIRED

8263 MULTIPLEXER — BIT 12 — (FROM EXTERNAL) TO BE ADDED LATER IF DESIRED

8263 MULTIPLEXER — BIT 16 — (FROM EXTERNAL) TO BE ADDED LATER IF DESIRED

8263 MULTIPLEXER — BIT 20 — (FROM EXTERNAL) TO BE ADDED LATER IF DESIRED

DIGITAL MULTIPLEXER (ONE SET PER DIGITAL INTERFACE)

8202 CLOCK RESET A

8202 B

8202 C

8202 D

BT22 A — τ = 500 nsec — 150pf 10K +5V

BT22 B — τ = 1 μsec — 300pf 10K +5V (TRIGGERABLE IF HIGH)

τ = 1 μsec 300pf 10K +5V — C

τ = 1 μsec 300pf 10K +5V — D

(TO BE WIRED AS NEEDED FOR 'PULSE' BITS)

CONTROL BIT PULSE MONOS

107 REC — 100Ω

109 XTR — 820Ω +5V

CONTROL BITS FROM WORD NUMBER "N"

CONTROL WORD LATCHES (EIGHT SETS PER DIGITAL INTERFACE)

24 SYS.

(TO OTHER CONTROL BIT LATCHES)

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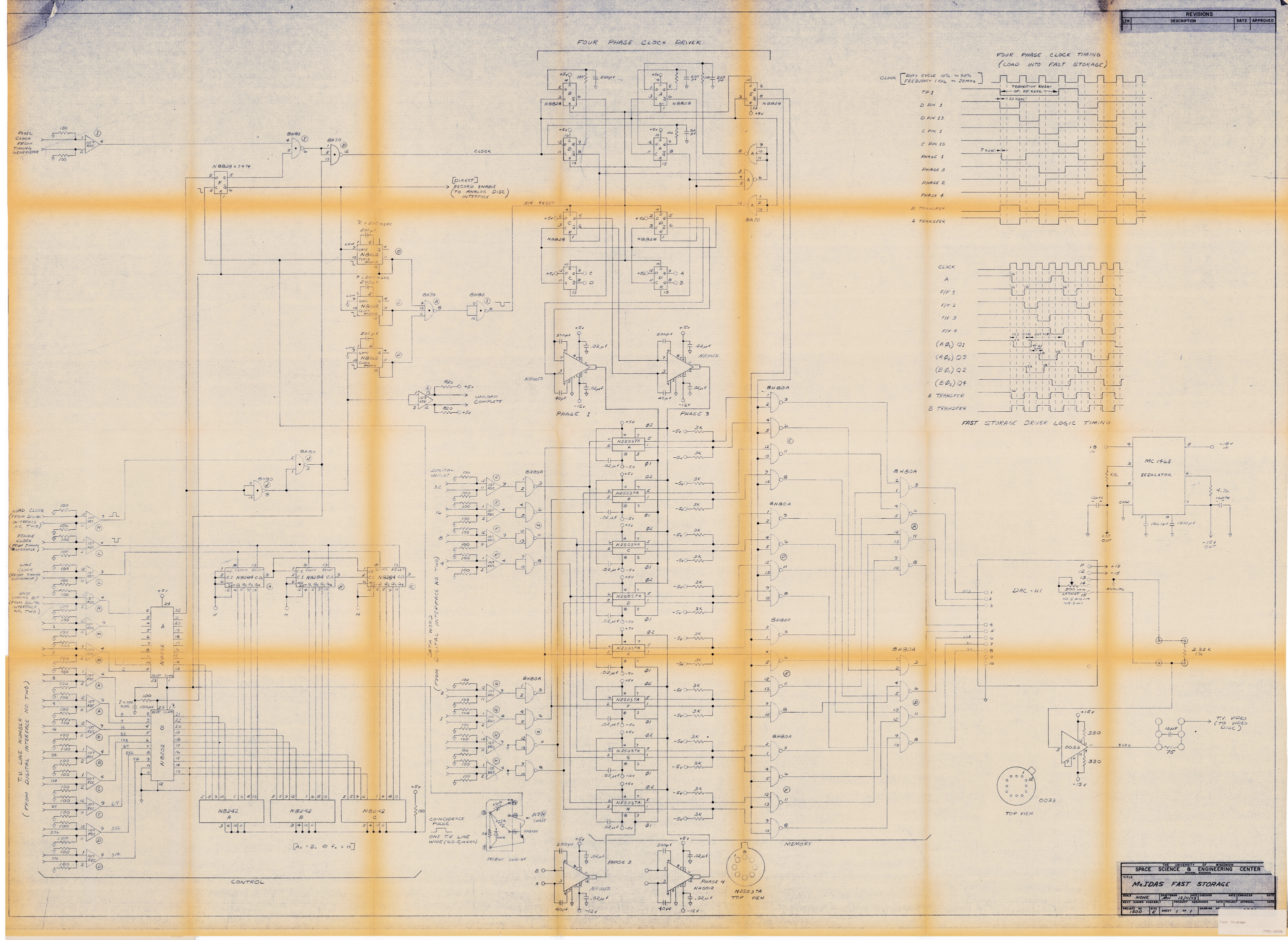
TITLE	McIDAS DIGITAL INTERFACE LATCH DETAIL
SCALE NONE	DRAFTSMAN Jeri 11/3/75
CHECKER	ENGINEER
NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE
PROJECT NO. 5010	SIZE E
SHEET 2 OF 2	DRAWING NO.

Digital Interface Latch Detail
7001-2005



REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
FOUR PHASE CLOCK DRIVER
FOUR PHASE CLOCK TIMING
(LOAD INTO FAST STORAGE)
CLOCK [DUTY CYCLE 10% TO 90% FREQUENCY 1 KHz TO 20 MHz]
TRANSITION DELAY OF 20 nsec
TP 1
D PIN 1
D PIN 13
C PIN 1
C PIN 13
PHASE 1
PHASE 3
PHASE 2
PHASE 4
B TRANSFER
A TRANSFER
CLOCK
A
F/F 1
F/F 2
F/F 3
F/F 4
(AØ1) Q1
(AØ2) Q3
(BØ1) Q2
(BØ2) Q4
A TRANSFER
B TRANSFER
FAST STORAGE DRIVER LOGIC TIMING
PIXEL CLOCK FROM TIMING GENERATOR
CLOCK
[DIRECT] RECORD ENABLE (TO ANALOG DISC INTERFACE)
SIR RESET
UNLOAD COMPLETE
PHASE 1
PHASE 3
PHASE 2
PHASE 4
MEMORY
MC 1468 REGULATOR
DAC-H1
ANALOG
T.V. VIDEO (TO VIDEO DISC)
TOP VIEW
0033
N2503TA TOP VIEW
DIGITAL WEIGHT
DATA WORD (FROM DIGITAL INTERFACE NO. TWO)
LOAD CLOCK (FROM DIGITAL INTERFACE NO. TWO)
FRAME CLOCK (FROM TIMING GENERATOR)
LINE CLOCK (FROM TIMING GENERATOR)
END LOADING BIT (FROM DIGITAL INTERFACE NO. TWO)
T.V. LINE NUMBER (FROM DIGITAL INTERFACE NO. TWO)
COINCIDENCE PULSE
ONE T.V. LINE WIDE (63.5 μsec)
PREVENT LOCK-UP
CONTROL
[Ax = Bx ⇒ fx = H]
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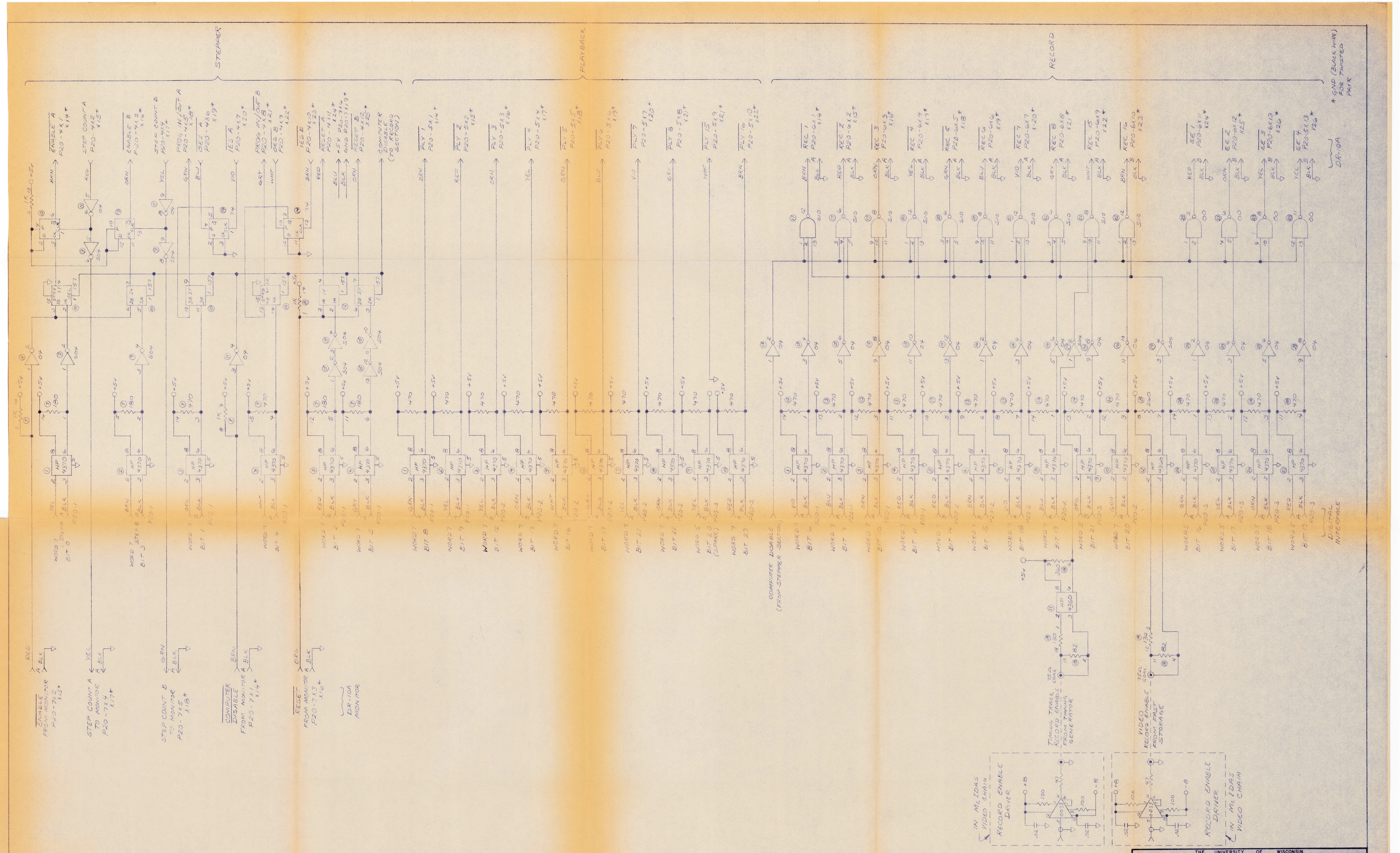
SPACE SCIENCE & ENGINEERING CENTER
MADISON, WISCONSIN
TITLE
McIDAS FAST STORAGE
SCALE NONE
DRAFTSMAN AW 12/11/73
CHECKER
ENGINEER
NEXT HIGHER ASSEMBLY
PRODUCT ASSURANCE
PROJECT APPROVAL
PROJECT NO. 1500
SIZE E
SHEET 1 OF 1
DRAWING NO.



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MADISON, WISCONSIN

TITLE: McIDAS DR-10A INTERFACE

SCALE	DRAFTSMAN	DATE	CHECKER	DATE	ENGINEER	DATE
NONE	[illegible]	4-2-75				

NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE	DATE	PROJECT ARROWAL	DATE

PROJECT NO.	SIZE	SHEET	OF	DRAWING NO.
7001	D	1	1	

DR-10A Interface

7001-2007

AUTO SWEEP SYSTEM

DISC SHUTDOWN SYSTEM

ULTRASONIC LEVEL DETECTOR

ON LINE

AUTO SWEEP (TO SHUTDOWN SYSTEM)

AUTO SWEEP DISCONNECT (FROM SHUTDOWN SYSTEM)

ENABLE (TO INTERFACE) P21-1X5 P21-1X15

INTERNAL +5 IND

RESET (TO INTERFACE) P21-1X3 P21-1X16

AUTO SWEEP

COMPUTER DISABLE (TO INTERFACE) P21-1X4 P21-1X14

N.O. ON LINE

INTERFACE +5 IND (TO INTERFACE) P21-1X6 P21-1X19

STEP COUNT A (FROM INTERFACE) P21-1X4 P21-1X17

STEP COUNT B (FROM INTERFACE) P21-1X5 P21-1X18

120VAC 60~

DR-10 POWER

TO DIAL-UP

AUTO SWEEP DISCONNECT

FROM ULTRASONIC LEVEL DETECTOR

FROM ULTRASONIC DETECTOR FAILURE

FROM DISC SLOW DOWN

FROM DETECTOR

TO SHUTDOWN SYSTEM (ULTRASONIC FAILURE)

TO SHUTDOWN SYSTEM (ULTRASONIC DETECTOR FAILURE)

RESTART N.O.

FRONT PANEL

CT (FRONT PANEL)

THE UNIVERSITY OF WISCONSIN SPACE SCIENCE & ENGINEERING CENTER MADISON, WISCONSIN			
TITLE: DR-10A DISC MONITOR			
SCALE: NONE	DRAFTSMAN: [illegible] DATE: 4-9-75	CHECKER: DATE:	ENGINEER: DATE:
NEXT HIGHER ASSEMBLY:	PRODUCT ASSURANCE: DATE:		
PROJECT NO.: 7001	SIZE: E	SHEET: 1 OF 1	DRAWING NO.:

DR-10A Disc Monitor

7001-2008

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

CHANNEL THREE ADDRESS MUX A (TIMING UNIT)
[FROM ADDRESS

THIS SECTION NOT USED 3-18-75

CHANNEL THREE ADDRESS MUX B (TIMING UNIT)
[FROM ADDRESS

P*-5 ORG/BLK — 107 REC — X
P*-5 YEL/BLK — 107 REC — ZZ
P*-5 WHT/BLK — 107 REC — Z
P*-5 BRN/BLK — 107 REC — Y
P*-5 SL/BLK — 107 REC — W
P*-5 VIO/BLK — 107 REC
P*-5 BLU/BLK — 107 REC
P*-5 GRN/BLK — 107 REC

WRITE ENABLE B (FROM DIGITAL INTERFACE NO. ONE)

WRITE ENABLE

BIT 00 ADDRESS
01
10
11
3
4
5
6

P3101A WE CS A_0 A_1 A_2 A_3 D_1 D_2 D_3 D_4 O_1 O_2 O_3 O_4
A
B
C
D
E
F
G
H

+5v — 300Ω

BIT 2
BIT 1 (MSB)

OUTPUT DATA

TO CHANNEL TWO

CHANNEL TWO LOOK-UP TABLE

P*-5 ORG/BLK — 107 REC — A
P*-5 YEL/BLK — 107 REC — B
P*-5 BRN/BLK — 107 REC — C
P*-5 RED/BLK — 107 REC — D
P*-4 YEL/BLK — 107 REC — E
P*-4 ORG/BLK — 107 REC — F
P*-4 RED/BLK — 107 REC — G
P*-4 BRN/BLK — 107 REC — H

CHANNEL THREE WRITE ENABLE P*-6 ORG/BLK (FROM DIGITAL INTERFACE NO. ONE)

WRITE ENABLE

NOT USED IN AECRL

BIT 6 (LSB)
BIT 5
BIT 4
BIT 3

CHANNEL THREE LOOK-UP TABLE

P*-4 SL/BLK — 107 REC — F
P*-4 VIO/BLK — 107 REC
P*-4 BLU/BLK — 107 REC — G
P*-4 GRN/BLK — 107 REC
P*-4 YEL/BLK — 107 REC — H
P*-4 ORG/BLK — 107 REC
P*-4 RED/BLK — 107 REC — I
P*-4 BRN/BLK — 107 REC — E

WRITE ENABLE A P*-6 RD/BLK (FROM DIGITAL INTERFACE NO. ONE)

WRITE ENABLE

CHANNEL ONE LOOK-UP TABLE

BIT 1 MSB
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6 LSB

P*-3 ORG/BLK — 107 REC — J
P*-3 YEL/BLK — 107 REC
P*-3 RD/BLK — 107 REC — K
P*-3 BRN/BLK — 107 REC
P*-3 SL/BLK — 107 REC — L
P*-3 WHT/BLK — 107 REC

INPUT ENHANCEMENT DATA (FROM DIGITAL INTERFACE NO. ONE)

NOTES
1. P*-4 THE * IMPLIES THE FOLLOWING:
   6 IMPLIES RED
   5 IMPLIES GREEN
   4 IMPLIES BLUE
2. ALL UNMARKED RESISTORS HAVE A VALUE OF 100 Ω.

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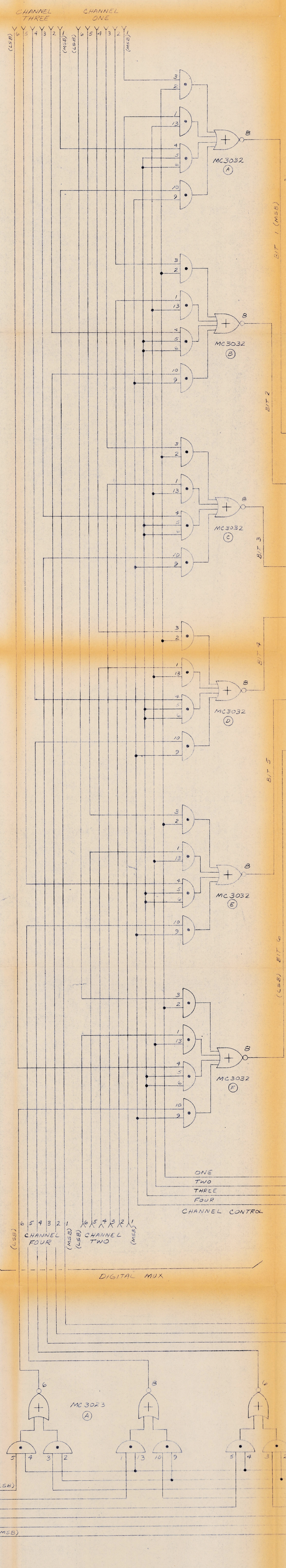
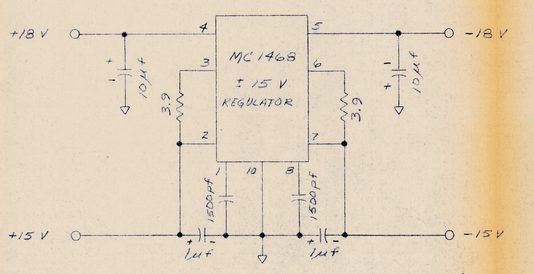
TITLE: McIDAS RED GREEN BLUE ENHANCEMENT TABLE					
SCALE NONE	DRAFTSMAN JGW 10/29/73	CHECKER	DATE	ENGINEER	DATE
NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE				
PROJECT NO. 1500	SIZE E	SHEET 1 OF 2	DRAWING NO.		

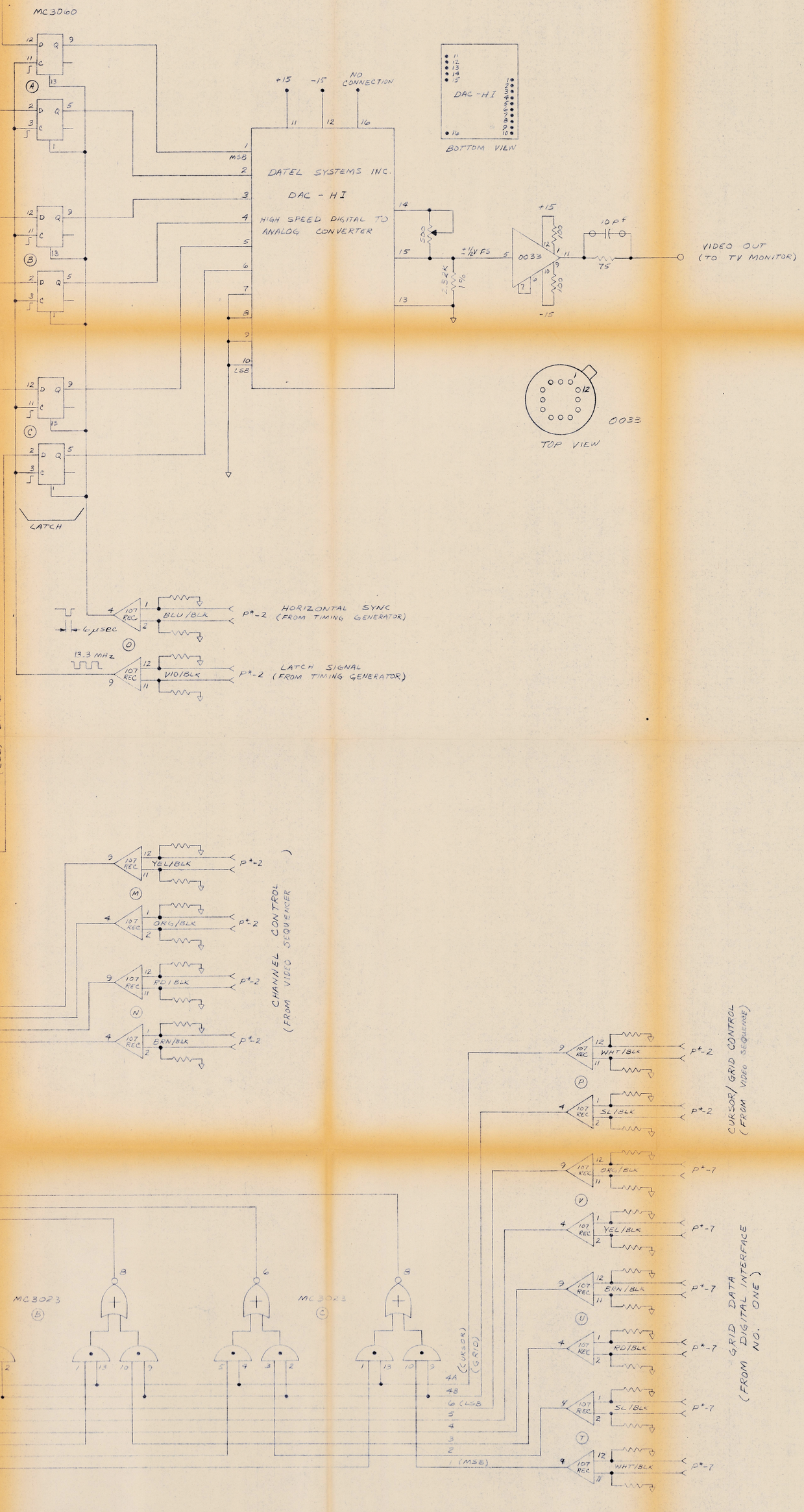
ENHANCEMENT TABLE
(2 Drawing Set)

7001-2009

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED







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TITLE: McIDAS RED GREEN BLUE ENHANCEMENT TABLE			
SCALE: NONE	DRAFTSMAN: JRW 10/24/73	CHECKER: DATE	ENGINEER: DATE
NEXT HIGHER ASSEMBLY	PRODUCT ASSURANCE: DATE		
PROJECT NO. 1500	SIZE E	SHEET 2 OF 2	DRAWING NO.

ENHANCEMENT TABLE
(2 Drawing Set)

7001-2009